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NOTICE OF ALLOWANCE AND FEE(S) DUE

181 7590 12/16/2008

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER

HARRISON, MONICA D

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 03/16/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,785	09/06/2005	Yoshihiko Shimauki	XA-10255	3053
TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/16/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE** OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

181 7590 12/16/2008

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

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10/519,785	09/06/2005	Yoshihiko Shimamuki	XA-10255	3053

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nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/16/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2893	257-678000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
 Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833			HARRISON, MONICA D	
			ART UNIT	PAPER NUMBER
			2893	

DATE MAILED: 12/16/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 618 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 618 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability**Application No.**

10/519,785

Applicant(s)

SHIMANUKI ET AL.

Examiner

Monica D. Harrison

Art Unit

2893

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 7/17/08.
2. ☒ The allowed claim(s) is/are 1-32.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date 2/7/07 and 6/9/08
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-4 and 6-26 in the reply filed on 7/17/08 is acknowledged.
2. Claims 1-4 and 6-26 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(B), claims 5 and 27-32, directed to the process of making or using an allowable product, previously withdrawn from consideration as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because all claims previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, **the restriction requirement as set forth in the Office action mailed on 6/17/08 is hereby withdrawn.** In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

3. Claims 1-32 are allowed over the prior art of record.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance: The prior art does not disclose nor fairly suggest a semiconductor device which has a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein a length between inner ends of said sealing-portion forming surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces (claim 1), a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein a length between inner ends of said sealing-portion forming surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces, and a notch portion is formed in the inner end of said sealing-portion forming surface (claim 2), a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein a length between inner ends of said sealing-portion forming surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces, and at least one portion of said sealing-portion forming surface is larger in width than said mounted surface (claim 3), a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein a length between inner ends of said sealing-portion forming surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces, and at least one portion of said sealing-portion forming surface is larger in width than said mounted surface (claim 4), a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein each of said leads is formed so that a length between inner ends of said sealing-portion forming

surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces, and each of said leads has said sealing-portion forming surface wider than said mounted surface (claim 6), a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein a length between inner ends of said sealing- portion forming surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces, said tab is formed to be smaller than a main surface of said semiconductor chip, and a portion of said sealing portion is disposed on a side of a rear surface which is an opposite surface to a chip mounting side of said tab (claim 11), a plurality of wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein a length between inner ends of said sealing- portion forming surfaces of said leads disposed to oppose to each other is longer than a length between inner ends of said mounted surfaces, said tab is formed to be smaller than a main surface of said semiconductor chip, and a portion of said sealing portion is disposed on a side of a rear surface which is an opposite surface to a chip mounting side of said tab, and a length projecting from an end portion of said tab of said semiconductor chip is shorter than a length directed to a lead-extending direction of said mounted surface of said lead (claim 15), a plurality of conductive wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein the conductive wires, whose one ends are connected to the surface electrodes of said semiconductor chip, are such that the other ends thereof are connected to a region opposing to said mounted surface of an opposite surface to said mounted surface of said hanging lead (claim 16), a plurality of conductive wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein the conductive wires, whose

one ends are connected to an electrode for GND among the surface electrodes of said semiconductor chip, are such that the other ends thereof are connected to a region opposing to said mounted surface of an opposite surface to said mounted surface of said hanging lead (claim 21), a plurality of conductive wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto, wherein the conductive wires, whose one ends are connected to the surface electrodes of said semiconductor chip, are such that the other ends thereof are connected to a region opposing to said mounted surface of an opposite surface to said mounted surface of said hanging lead, and a length of said mounted surface in an extending direction of said hanging lead is larger than a thickness of said hanging lead on said mounted surface (claim 23), a plurality of conductive wires for connecting surface electrodes of said semiconductor chip and said sealing-portion forming surfaces corresponding thereto, wherein said leads are formed so that a length between inner ends of said sealing-portion forming surfaces of said leads disposed to oppose to each other is larger than a length between inner ends of said mounted surfaces of said leads, and the conductive wires, whose one ends are connected to the surface electrodes of said semiconductor chip, are such that the other ends thereof are connected to a region opposing to said mounted surface of an opposite surface to said mounted surface of said hanging lead (claim 26) and a plurality of conductive wires for connecting surface electrodes of said semiconductor chip and said leads corresponding thereto; and a conductive wire for connecting a surface electrode for GND of said semiconductor chip and said hanging lead, the method comprising the step of: testing said semiconductor device with a GND potential being supplied to a desired circuit of said semiconductor chip through a lead for GND among said plurality of leads and said hanging lead (claim 32) nor the method of manufacturing a

semiconductor device which connecting surface electrodes of said semiconductor chip and said sealing portion forming surfaces corresponding thereto by wires; resin-sealing said semiconductor chip, said sealing-portion forming surfaces, and said plurality of wires, and forming a sealing portion that the mounted surfaces of said plurality of leads are exposed to and arranged on a peripheral portion of a rear surface; and cutting each of said leads and separating it from said lead frame (claim 5), connecting surface electrodes of said semiconductor chip and said sealing portion forming surfaces corresponding thereto by conductive wires; performing resin molding with said plurality of device regions being covered with one cavity of a resin molding die, and forming a batch sealing portion so that the mounted surfaces of said plurality of leads are exposed to and arranged on a peripheral portion of a rear surface; and clipping said sealing-portion forming surface and said mounted surface of each of said leads by a cutting die, cutting each of the leads and said batch sealing portion by dicing, and separating them from said lead frame (claim 27), connecting a surface electrode of said semiconductor chip and a portion located inside said concave portion in said sealing-portion forming surface of said lead corresponding thereto by a conductive wire; disposing a film on a die surface of a resin molding die, performing die clamping with said plurality of device regions being covered with one cavity of the resin molding die, making said mounted surface of said lead intrude into said film by said die clamping to perform resin molding, and thereby forming a batch sealing portion so that the mounted surfaces of said plurality of leads are exposed to and arranged on a peripheral portion of a rear surface; and cutting each of the leads and said batch sealing portion by dicing, and separating them from said lead frame (claim 28) and connecting a surface electrode of said semiconductor chip and said sealing-portion forming surface in a region located inside said stress

relaxing means of said lead corresponding thereto by a conductive wire; resin-sealing said semiconductor, said sealing forming surfaces, and said plurality of wires, and forming a sealing portion so that the mounted surfaces of said plurality of leads are exposed to and arranged on a peripheral portion of a rear surface; and cutting each of said leads by a punch in a state in which a portion located outside said stress relaxing means of each of said leads is clipped by a cutting die, and separating it from said lead frame (claim 29) and in the context of their recited apparatus and process along with their depending claims.

The prior art discloses that it is difficult to mount larger semiconductor chips without changing the package size. However, the applicants invention discloses a chip mounting region surrounded by the inner end of the sealing-portion forming surface of each lead which can be expanded and the size of the mountable chip is increased which clear up the deficiencies in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2893

mdh
December 2, 2008

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893